Connecting the Smart LCD to the Intel® PXA27x Processor

Application Note

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1.0 Introduction

A smart panel is an LCD panel that contains an internal frame buffer memory. The smart panel uses its internal frame buffer memory to refresh the display. Panels without an internal frame buffer are referred to as “non-smart” panels. An external processor updates the smart panel’s internal frame buffer memory only when the display is to be changed. In a mobile phone system, a smart panel can be used as the main panel as well as the secondary panel. On secondary smart panels, smart phones can implement not only Call Link Information (CLI), but advanced features such as camera capture preview, soft keypad display, and media file playback information.

Figure 1. Block Diagram of the Intel® PXA27x Processor

Figure 1 is a block diagram of the Intel® PXA27x Processor (PXA27x processor). The PXA27x processor LCD controller has direct communication with the PXA27x system bus. At the same time, the LCD controller has a versatile interface that can host different kinds of panels. The LCD controller is backward-compatible with both the Intel® PXA25x and the Intel® PXA26x LCD controllers. The types of LCD panels that are supported include:

- Single- or dual-scan display modules
- Up to 256 gray-scale levels (8 bits) in passive monochrome mode
2.0 Intel® PXA27x Processor Smart LCD Interface

To interface to a smart panel, the PXA27x processor uses the same physical pins as used with a normal LCD panel, but with several additional pins. See Table 1 for a description of the pins and their functions.

2.1 Available Signals

Table 1. Intel® PXA27x Processor Smart Panel Interface Signals

<table>
<thead>
<tr>
<th>Intel® PXA27x Pin</th>
<th>Panel Pin</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDD&lt;7:0&gt;</td>
<td>D&lt;7:0&gt;</td>
<td>Output</td>
<td>8-bit data lines used to transmit data values to a smart panel</td>
</tr>
<tr>
<td>L_PCLK_WR</td>
<td>Write</td>
<td>Output</td>
<td>Write signal to a smart panel</td>
</tr>
<tr>
<td>L_LCLK_A0</td>
<td>Command/DATA</td>
<td>Output</td>
<td>This control signal specifies command or data transaction: 0 = Command transaction 1 = Data transaction</td>
</tr>
<tr>
<td>L_FCLK_RD</td>
<td>Read</td>
<td>Output</td>
<td>Read signal to a smart panels.</td>
</tr>
<tr>
<td>L_CS</td>
<td>Chip Select</td>
<td>Output</td>
<td>Used as a chip-select signal for a smart panel. 0 = Selected 1 = Unselected</td>
</tr>
<tr>
<td>L_VSYNC</td>
<td>Sync</td>
<td>Input</td>
<td>Refresh sync signal from the LCD panel.</td>
</tr>
</tbody>
</table>

NOTES:
1. Names used for smart panel pin are representative names and do not match those on all smart panels. Similarly, not all signals are required for all modes of operation. Refer to the smart panel reference documentation for relative detailed information.
2. In reference to the Intel® PXA27x processor, outputs are pins that drive a signal from the Intel® PXA27x processor to another device.
2.2 Data Format

The PXA27x processor smart panel interface uses only eight data pins (LDD<7:0>). Therefore, data from the PXA27x processor LCD controller output FIFO is driven onto the 8-bit-wide bus in three cycles as shown in Figure 2. The data width for each color (red, green, and blue) can be 5 bits, 6 bits, 7 bits, or 8 bits, depending on pixel depths and format.

Figure 2. Intel® PXA27x Processor 8-Bit Data Interface for Smart Panels

<table>
<thead>
<tr>
<th>LDD&lt;7&gt;</th>
<th>LDD&lt;6&gt;</th>
<th>LDD&lt;5&gt;</th>
<th>LDD&lt;4&gt;</th>
<th>LDD&lt;3&gt;</th>
<th>LDD&lt;2&gt;</th>
<th>LDD&lt;1&gt;</th>
<th>LDD&lt;0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel0 Red Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pixel0 Green Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pixel0 Blue Data</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For example, if the data format for a smart panel is 16 bpp in RGB 5:6:5 mode, the pixel data is output using 3 bytes. Table 2 shows the byte order and bit order.

Table 2. Data Format for 16bpp RGB 5:6:5

<table>
<thead>
<tr>
<th>LDD&lt;7&gt;</th>
<th>LDD&lt;6&gt;</th>
<th>LDD&lt;5&gt;</th>
<th>LDD&lt;4&gt;</th>
<th>LDD&lt;3&gt;</th>
<th>LDD&lt;2&gt;</th>
<th>LDD&lt;1&gt;</th>
<th>LDD&lt;0&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>R4</td>
<td>R3</td>
<td>R2</td>
<td>R1</td>
<td>R0</td>
<td>R4 &amp; R3 &amp; R2 &amp; R1 &amp; R0</td>
<td>R4 &amp; R3 &amp; R2 &amp; R1 &amp; R0</td>
<td>R4 &amp; R3 &amp; R2 &amp; R1 &amp; R0</td>
</tr>
<tr>
<td>G5</td>
<td>G4</td>
<td>G3</td>
<td>G2</td>
<td>G1</td>
<td>G0</td>
<td>G5 &amp; G4 &amp; G3 &amp; G2 &amp; G1 &amp; G0</td>
<td>G5 &amp; G4 &amp; G3 &amp; G2 &amp; G1 &amp; G0</td>
</tr>
</tbody>
</table>

Note: Refer to the smart-panel manufacturer specifications for how data is transmitted to the corresponding display, and ensure that it complies with the PXA27x processor smart-panel data format.

2.3 Commands

When programming a panel, the software driver deals with two types of commands. The first type is the command for the LCD controller itself; the second type, for the smart panel. Different types of smart panels may define different command sets. Refer to the corresponding smart-panel specification for details. The PXA27x processor LCD controller sends a command to a smart panel by executing a Command Write command.

Note: This document discusses only commands for the PXA27x processor LCD controller, as defined in the Intel® PXA27x Processor Family Developer’s Manual. DMA channel 6 moves smart-panel commands from system memory to the command FIFO in the LCD controller, and the LCD controller then executes those commands.

For details on the following bullets, refer to the Intel® PXA27x Processor Family Design Guide and the Intel® PXA27x Processor Family Developer’s Manual.
2.4 Smart LCD

2.4.1 Available Signals

Different smart LCD panels can have different definitions for signal pins. This application note provides only a general description of these signal pins. Refer to Section 2.1 for details as well as the datasheet of the smart panel being used.

2.4.2 Smart LCD Command Sets

Different smart panels define different command sets. For details, refer to the datasheet of the smart panel being used. Typical commands provide functionalities such as:

- Sleep in/Sleep out: Places the smart panel in/out of sleep mode for power control.
- Display on/off: Turns on/off the smart panel.
- Display mode setting: Contrasts level, color temperature, etc.
- Simple graphic commands: Draws line, draws rectangle, scrolls, etc.

A smart panel must be set correctly using the setting commands before it can display properly.

3.0 Connecting a Smart Panel to the Intel® PXA27x Platform

3.1 Connection

Figure 3 shows how to connect smart-panel pins to the PXA27x processor LCD controller signals.

D<0-7>: Data lines of the smart panel are connected directly to the PXA27x processor LCD data signals – LDD<0-7>. All of the commands and data are transferred between the PXA27x processor and the smart panel via these eight data lines. Before beginning a design, refer to Section 2.2 for details on the data format of the PXA27x processor smart-panel interface.

SELECT: Smart-panel chip-select signal is connected to the PXA27x processor L_CS pin, which is designed to generate a select signal for smart panels.
COMMAND: COMMAND pin of the smart panel is connected to the PXA27x processor L_LCLK_A0 pin to identify data and command information sent from the PXA27x processor to the smart panel on the 8-pin data bus.

WRITE: Smart-panel write strobe pin is connected to the PXA27x processor L_PCLK_WR signal.

READ: Smart-panel read strobe pin is connected to the PXA27x processor L_FCLK_READ signal.

SYNC: If a smart panel has a SYNC signal, connect it to the PXA27x processor L_VSYNC signal.

Figure 3. Connection Between the Intel® PXA27x Processor and Smart Panel

3.2 Typical Usage

Smart panels are used widely in cell phone systems. Several possible usage models include:

- A smart panel as the sole panel of the phone
- A standard LCD as the main panel and a smart panel as the secondary panel
- Two smart panels as main and secondary panel

3.2.1 One Smart LCD

Some phone systems have only one smart panel that functions as the main LCD panel of the system. The PXA27x processor does not have to constantly refresh the LCD because the smart panel can maintain the latest frame within its internal frame buffer. This saves PXA27x processor system bus and memory bus bandwidth. At the same time, the PXA27x processor can be placed into low-power mode (sleep, idle, and so on) to save power consumption if there is no need to refresh the display content. Refer to Figure 3 for connection details.
3.2.2 One Normal LCD and One Smart LCD

This is one of most popular combinations of a standard LCD panel and a smart panel, often seen in flip-phone systems. The standard LCD panel acts as the main panel when the lid is open, and the smart panel acts as a secondary panel when the lid is closed. Most of the LCD signals can be shared between the standard LCD panel and the smart panel as shown in Figure 4.

Figure 4. Typical Usage of Standard LCD Panel and Smart LCD Panel

GPIOx is used to switch L_PCLK_WR between the main LCD panel and the secondary smart LCD panel. When the PXA27x processor must refresh the main panel, there is no WRITE signal for the smart panel. However, the smart panel can continue displaying content from its internal frame buffer, if preferred. When the PXA27x processor refreshes the internal frame buffer of the smart panel, nothing can be displayed on the standard LCD panel.

The decoder in Figure 4 is used to eliminate impact on the standard LCD when the PXA27x processor refreshes the smart LCD panel. However, the decoder is not needed if the standard LCD is powered off when the smart panel is being refreshed.

3.2.3 Two Smart LCD Panels

In some phone systems, two smart LCD panels are used. One serves as the main panel and the other serves as the secondary panel. As shown in Figure 5, two GPIO pins are used to enable one of the panels for refresh from the processor while the other panel displays content from its internal frame buffer. This use can save PXA27x system bus and memory bus bandwidth, as well as related power consumption.
4.0 Smart LCD Driver

A Smart LCD panel driver has been implemented in Linux. The following subsections describe key operations that are common for all operating systems:

4.1 LCD Controller Register Setting

During boot-up, the PXA27x processor LCD controller is not enabled; that is, LCCR0[ENB] is not set. The driver enables the LCD controller each time before loading a command to the LCD controller, and disables it when all commands has been loaded and executed.

A Wait-for-Sync command is inserted at the end of a command sequence so that the LCD controller stops when all commands before this command are executed:

```
CMDCR[SYNC_CNT] = 0x1; //Wait for one L_VSYNC signal to be asserted.
```

When sending pixels data using a Data Write command, do not be concerned about pixel format settings, such as LCCR3[PDFOR], LCCR3[BPP]. The driver reads data from an input pixel buffer and sends that data to the smart panel. If using a Frame Data Write command to transfer pixel data, the register settings shown in Figure 6 take effect.
A0CSRD_SET = A0 and CS Setup Time before L_FCLK_RD is asserted
A0CSRD_HLD = A0 and CS Hold Time after L_FCLK_RD is deasserted
A0CSWR_SET = A0 and CS Setup Time before L_PCLK_WR is asserted
A0CSWR_HLD = A0 and CS Hold Time after L_PCLK_WR is deasserted
WR_PULWD = L_PCLK_WR pulse width
RD_PULWD = L_FCLK_RD pulse width
DWR_SET = Data Setup Time before L_PCLK_WR is asserted
DWR_HLD = Data Hold Time after L_PCLK_WR is deasserted
CMD_INH = Command Inhibit time between two writes

Note: The latency between two writes (L_PCLK_WR high to next L_PCLK_WR low) is the larger of

\[(\text{CMD\_INH} = (\text{PCD} + 1) \times \text{LCDCLK})\] or
\[(\text{A0CSWR\_SET} + \text{A0CSWR\_HLD} + 2 \times \text{LCDCLK})\]

where
\[\text{A0CSWR\_SET} = \text{A0CSWR\_HLD} = (\text{BLW} + 1) \times \text{LCDCLK}.\]

The pulse width of L_CS high is about two LCD clocks and cannot be adjusted.

The following registers select LCD controller timing in Smart LCD panel mode. Select the timing settings according to the timing requirements of the smart panel being used.

- LCCR1[BLW]: Pulse width of read and write signals (L_PCLK_WR and L_FCLK_RD).
Connecting the Smart LCD to the Intel® PXA27x Processor

4.2 Load Commands

At boot-up, the driver allocates a command buffer. The commands that are to be loaded to the PXA27x processor LCD controller are filled into the buffer. The commands are then loaded from the command buffer to the LCD controller internal FIFO using DMA channel 6 of the LCD controller. To ensure that the LCD controller has executed all loaded commands as expected (no more and no less), two synchronization commands are inserted at the end of the commands:

Interrupt Processor: Set LCSR0_CMD_INT bit when executed

Wait for Vsync: Stops the LCD controller from executing next command

The command loading sequence is:

```c
PRSR |= PRSR_ST_OK | PRSR_CON_NT; //Continue to execute next command
FDADR6 = fdadr6; //Set up DMA 6 to transfer Command
LCCR0 |= LCCR0_ENB; // Begin sending
while ((LCSR0 & LCSR0_CMD_INT) == 0); //Wait until the last command is executed.
// Quick disable
PRSR &= ~(PRSR_ST_OK | PRSR_CON_NT);
LCCR0 &= ~(LCCR0_ENB);
LCSR0 |= LCSR0_CMD_INT; // Clear CMD_INT
FDADR6 = 0; // Disable DMA 6
```

4.2.1 Update Display

The display can be updated in two ways. Choose the proper method based on the LCD panel interface.

- Write display data to the smart LCD panels internal buffer byte by byte (and pixel by pixel) using the Data Write command. Pixel data is wrapped in this command as:

  ```c
  cmd = LCD_CMD_DATA_WRITE | LCD_CMD_A0_DATA | pixel_data_byte;
  ```
This method can be used for smart panels that do not conform to the PXA27x processor 8-bit-wide-bus-in-three-cycles interface. Software must read each pixel from the frame buffer, wrap it into a Data Write command, and put it into the command buffer. As a result, performance may be reduced. Also, it would be difficult to display overlays using this method.

- Write a whole frame of display data to the smart LCD panel internal buffer using a single Frame Data Write command. The sequence is:

  Set up FDADRx for base plane and overlays;

  Execute Frame Data Write command:

  ```
  LCD_CMD_FRAME_DATA_WRITE | LCD_CMD_A0_DATA;
  FDADRx = 0;
  ```

The smart LCD panel has to conform to the PXA27x processor LCD controller 8-bit-wide-bus-in-three-cycles interface. When using this command, pixel data is transferred using DMA channels of the LCD controller. Hardware handles pixel data conversion and combination so that overlays can be enabled.

**Note:** The Frame Data Write format definition (Table 7-23) in the *Intel® PXA27x Processor Family Developer’s Manual* does not specify that the A0 bit should be set to 0b1, while this bit is important.

For this usage model, invoke a screen update from the application or update it within the driver at certain intervals (for example, using a timer).

### 5.0 Summary

This application note provides basic information for smart panels (including secondary panels) and considerations for the hardware connection between a smart panel and the PXA27x processor LCD controller. The versatility of the PXA27x processor smart panel interface can easily handle implementing Call Link information, camera-capture preview, soft keyboard display, and media-file playback information.